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(54) Amplifier circuit

(57) A balanced type DDA 1 is combined with a single end type DDA 2 to form a differential amplifier circuit 3 which is a balanced type DDA. The balanced type DDA 1 has four input terminals VPP, VPN, VNN and VNP which are input terminals of two differential input stages, and two output terminals VoutP and VoutN which are output terminals of two output stages. These terminals are four input terminals and two output terminals of the differential amplifier circuit 3. The single end type DDA 2 has four input terminals, which are input ter-

minals of two differential input stages and which are connected to the four input terminals of the differential amplifier circuit 3, respectively. The single end type DDA 2 also has an output terminal vout of one output stage, which serves as a control output terminal for the feedback control of the differential amplifier circuit 3. By the negative feedback of the signal of the control output terminal Vout, a virtual short-circuit can be established between two input terminals of each differential input stages, so that it is possible to reduce distortion without reducing gains.

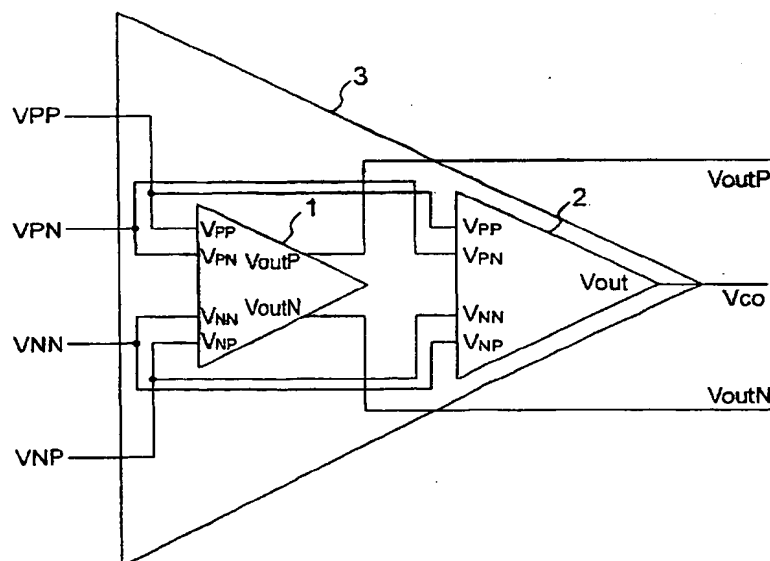


FIG. 8

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AM

Description

BACKGROUND OF THE INVENTION5 Field of The Invention

[0001] The present invention relates generally to a fully differential type amplifier circuit using a differential difference amplifier (DDA).

10 Description of The Related Background Art

[0002] Conventionally, in order to form a non-inverting amplifier having large input impedance, a technique based on a fully differential type (balanced type) DDA is employed. The balanced type DDA is shown in a symbolic diagram of FIG. 1 and in a circuit diagram of FIG. 2. This DDA 1 includes: a differential input stage 11 comprising NMOS transistors Q1, Q2 and Q13; a differential input stage 12 comprising NMOS transistors Q3, Q4 and Q15; an output stage 13 having a PMOS transistor Q11 and an NMOS transistor Q14; an output stage 14 having a PMOS transistor Q12 and an NMOS transistor Q16; four input terminals VPP, VPN, VNP and VNN; and two output terminals VoutP and VoutN.

[0003] Between the output terminals VoutN and VoutP, a common mode feedback circuit 15 is provided. The common mode feedback circuit 15 controls the gate voltages of PMOS transistors Q5 and Q6 which are used as common loads to the two differential input stages 11 and 12. The connection node of the transistors Q5, Q2 and Q3 controls the gate of one output stage transistor Q12, and the connection node of the transistors Q6, Q4 and Q1 controls the gate of the other output stage transistor Q11.

[0004] A resistor R11 and a capacitor C11, which are provided between the gate and drain of the output stage transistor Q11, constitute a phase compensator circuit. Similarly, a resistor R12 and a capacitor C12, which are provided between the gate and drain of the output stage transistor Q12, constitute a phase compensator circuit. The NMOS transistors Q13 through Q16 are current source transistors for controlling a bias current for each of the differential input stages 11 and 12, and are controlled by a voltage Vbias which is applied from the outside of the circuit.

[0005] The common mode feedback circuit 15 is designed to carry out a negative feedback control for suppressing a output common mode component. For example, the common mode feedback circuit 15 is formed as shown in FIG. 3. The common mode feedback circuit 15 of FIG. 3 includes: a differential input stage comprising NMOS transistors Q21, Q22 and Q23; and a load circuit comprising PMOS transistors Q24 and Q25 which are diode-connected. The gate of one transistor Q21 of the differential input stage is connected to output terminals VoutN and VoutP via resistors R21 and R22, respectively. By these resistors R21 and R22, a common mode component contained in output signals VoutN and VoutP of the balanced type DDA 1 is detected. This is compared with a reference voltage VAG applied to the gate of the other transistor Q22 and a control signal VC is generated. By this control signal VC, the negative feedback control of the DDA 1 is carried out, so that the output common mode voltage is substantially equal to the VAG.

[0006] In such a balanced type DDA 1 having four inputs and two outputs, the output signal of one output terminal VoutP has a positive gain with respect to an input signal of a difference between the input terminal VPP and the input terminal VPN, and the output signal of the other output terminal VoutN has a negative gain with respect thereto. In addition, one output terminal VoutP has a negative gain with respect to an input signal of a difference between the input terminal VNP and the input terminal VNN, and the other output terminal VoutN has a positive gain with respect thereto. These gains are determined by a product of the gain of the differential input stage by the gain of the output stage. Assuming that the mutual conductance of the MOS transistors Q1, Q2, Q3 and Q4 is gm, the drain-to-source conductance is gdsn, and the drain-to-source conductance of the MOS transistors Q5 and Q6 is gdsp, then, the gain of the differential input stage with respect to the differential input signal is gm / (gdsn + gdsp). Therefore, it can be seen that the mutual conductance of the differential transistor pair of the differential input stage is in proportion to the absolute value of the gain of the DDA 1.

[0007] Using such a balanced type DDA 1, a non-inverting amplifier circuit is formed as shown in FIG. 4. This circuit comprises resistors R1 through R3 in addition to the balanced type DDA 1, and outputs VoutP and VoutN with respect to VinP and VinN. Since a negative feedback is applied to the circuit by the resistors R1 through R3, the operation of this non-linear amplifier circuit satisfies the following formula (1) assuming that the gain of the balanced type DDA 1 is infinity.

$$(VPP - VPN) - (VNP - VNN) = 0 \quad (1)$$

[0008] Therefore, assuming that the resistance value of the resistor R3 is Ra and that the resistance value of the

resistors R1 and R2 is Rb, the gain A of this circuit is expressed by the following formula (2).

$$A = \{R_b + (R_a/2)\} / (R_a/2) \quad (2)$$

[0009] Assuming that the common mode component of the input voltages VinP and VinN is VCMi, the differential component thereof is Vi, the common mode component of the output voltages VoutP and VoutN is VCMO, and the differential output component thereof is Vo, then, the following relationships (3) through (7) are established.

$$V_{PP} = V_{CMi} + V_i \quad (3)$$

$$V_{NP} = V_{CMi} - V_i \quad (4)$$

$$V_{outP} = V_{CMO} + V_o \quad (5)$$

$$V_{outN} = V_{CMO} - V_o \quad (6)$$

$$V_o = A \cdot V_i \quad (7)$$

[0010] Since the input terminal of the balanced type DDA 1 is connected to the gate of the MOS transistor as shown in FIG. 2, no current flows into the input terminal in principle. Therefore, VPN and VNN are determined by the resistors R1 through R3 and the output voltages VoutP and VoutN as shown in the following formulae (8) and (9).

$$V_{PN} = V_{AG} + V_i \quad (8)$$

$$V_{NN} = V_{AG} - V_i \quad (9)$$

[0011] If VCMi ≠ VCMO, then VPP ≠ VPN and VNP ≠ VNN. That is, if the common mode component VCM of the input voltage of the DDA 1 is different from the common mode component VCMO of the output voltage, two signals inputted to the differential input stage have different voltages.

[0012] Referring to FIGS. 5 and 6, the operation of the differential input stage will be considered. The differential input stage of FIG. 5 comprises NMOS transistors Q51, Q52 and Q53. The gate potential of the NMOS transistor Q53 is controlled by a voltage Vbias so as to flow a desired bias current Ibias. It is herein assumed that the gate-to-source voltage of the MOS transistor Q51 is VGS1, the drain current thereof is ID1, the gate-to-source voltage of the MOS transistor Q52 is VGS2, and the drain current thereof is ID2. Assuming that the characteristics of the MOS transistors Q51 and Q52 can be expressed by $ID = K (V_{GS} - V_{TH})^2$ using a gate-to-source voltage VGS, a drain current ID, a threshold voltage VTH and a mutual conductance parameter K, then, the relationship between $\Delta V_i = V_{GS1} - V_{GS2}$ and $\Delta ID = ID1 - ID2$ is expressed by the following formula (10).

$$\Delta ID = \Delta V_i \cdot K \{2 I_{bias} / K - (\Delta V_i)^2\}^{1/2} \quad (10)$$

[0013] The relationship of the formula (10) is shown in FIG. 6. It can be seen from this figure that a range (a linear operation range of a differential input stage), in which ΔID varies substantially linearly with respect to ΔV_i , is inversely in proportion to K. If this range is not sufficiently large as compared with the difference between the voltages of two signals inputted to the differential input stage, distortion occurs.

[0014] Therefore, it is conventionally designed that the linear operation range of the differential input stage is sufficiently large. Assuming that the channel width of the MOS transistor is W and the channel length thereof is L, K is in proportion to W/L, so that the linear operation range of the differential input stage can be enlarged if the W/L is decreased.

[0015] However, in this method, as can be seen from FIG. 6, the mutual conductance ($\Delta I_D / \Delta V_i$) of the differential input stage decreases, so that there is a problem in that the gain of the DDA decreases. As a result, there are other problems in that it is not possible to obtain a desired high gain, or if it is required to provide a DDA having a large gain-bandwidth product (GB product), it is required to take measures to increase the number of gain stages, and if the number of gain stages is increased, it is difficult to carry out a phase compensation.

[0016] In addition, a multiple input circuit using the balanced type DDA 1 is shown in FIG. 7. This multiple input circuit comprises the balanced type DDA 1 and resistors R1 through R7. This circuit is designed to input V_{inPP} , V_{inNN} , V_{inPn} and V_{inNP} and output V_{outP} and V_{outN} . In this circuit, in accordance with a differential component v_{iN} between the input voltages V_{inPN} and V_{inNN} and a differential component V_{iP} between the input voltages V_{inPP} and V_{inNP} , a differential output $V_{outP} - V_{outN}$ determined by $V_{iP} - V_{iN}$ is obtained.

[0017] In this case, since a negative feedback is applied to the circuit by the resistors R1 through R4, the operation of the circuit satisfies the above described formula (1) assuming that the gain of the balanced type DDA 1 is infinity.

[0018] Therefore, if it is set that $R_3 = R_4 = R_a$, $R_1 = R_2 = R_b$, $R_5 = R_6 = R_c$ and $R_7 = R_d$, assuming that the differential component between the input voltages V_{inPN} and V_{inNN} is V_{iN} and that the differential component between the input voltages V_{inPP} and V_{inNP} is V_{iP} , the differential output component V_o of the output voltages V_{outP} and V_{outN} of this circuit is expressed by the following formula (11).

$$V_o = \frac{(R_d / 2)(R_a + R_b)}{(R_c + R_d / 2)R_a} V_{iP} - \frac{R_b}{R_a} V_{iN} \quad (11)$$

[0019] Assuming that the common mode component of the input voltages V_{inPN} and V_{inNN} is V_{CMN} , the common mode component of the input voltages V_{inPP} and V_{inNP} is V_{CMP} , the differential component of the output voltages V_{outP} and V_{outN} is V_o , and the common mode component thereof is V_{CMO} , then, V_{PP} and V_{PN} are expressed by the following formulae (12) and (13), respectively.

$$V_{PP} = \frac{R_d / 2}{R_c + R_d / 2} V_{iP} + V_{CMP} \quad (12)$$

$$V_{PN} = \frac{(R_d / 2)V_{iP}}{R_c + R_d / 2} + \frac{R_b \cdot V_{CMN}}{R_a + R_b} + \frac{R_a \cdot V_{CMO}}{R_a + R_b} \quad (13)$$

[0020] It can be seen from these formulae that $V_{PP} \neq V_{PN}$ in general. The other pair of input voltages V_{NP} and V_{NN} are the same. That is, in the multiple input circuit shown in FIG. 7 similar to FIG. 4, two input signals to the differential input stage have different voltages to cause distortion. In order to solve this problem, it is required to enlarge the linear operation range of the balanced type DDA 1, so that the same problem as that in FIG. 4 is caused.

[0021] As described above, there are problems in that if the conventional balanced type DDA comprises a linear amplifier circuit and a multiple input circuit, distortion occurs, that if the linear operation range is intended to be enlarged in order to reduce distortion, the gain reduces, and that if the number of gain stages is increased to compensate this, it is difficult to carry out a phase compensation.

SUMMARY OF THE INVENTION

[0022] It is therefore an object of the present invention to eliminate the aforementioned problems and to provide an amplifier circuit capable of reducing distortion without reducing gains.

[0023] It is another object of the present invention to provide a non-inverting amplifier circuit and a multiple input circuit, which use such an amplifier circuit.

[0024] According a first aspect of the present invention there is provided an amplifier circuit comprising:

a first four-input balanced amplifier having

a first differential terminal pair and a second differential terminal pair;

a first output terminal and a second output terminal, output signals at the first output terminal and the second output terminal being complementary; and

a second four input single-ended amplifier having

a third differential terminal pair and a fourth differential terminal pair;

a third output terminal;

wherein the first differential terminal pair and the third differential terminal pair are connected in parallel, and the second differential terminal pair and the fourth differential terminal pair are connected in reverse parallel.

[0025] According a second aspect of the present invention there is provided an amplifier circuit comprising:

a first four-input balanced amplifier having
a first differential terminal pair and a second differential terminal pair;
a first output terminal and a second output terminal, output signals at the first output terminal and the second output terminal being complementary; and
a second four input single-ended amplifier having
a third differential terminal pair and a fourth differential terminal pair;
a third output terminal;
wherein the first differential terminal pair and the third differential terminal pair are connected in reverse parallel, and the second differential terminal pair and the fourth differential terminal pair are connected in parallel.

[0026] According to the present invention, a balanced type DDA, to which input terminals are commonly connected, is combined with a single end type DDA, so that the output terminal of the single end type DDA serves as a control output terminal. By carrying out a negative feedback control on the basis of the output of the control output terminal, a virtual short-circuit can be established between first and second input terminals and between third and fourth input terminals. Therefore, it is possible to reduce distortion without reducing gains.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The present invention will be understood more fully from the following detailed description and from the accompanying drawings of the preferred embodiments of the invention. However, the drawings are not intended to imply limitation of the invention to a specific embodiment, but are for explanation and understanding only.

[0028] In the drawings:

FIG. 1 is a symbolic diagram of a balanced type DDA;
FIG. 2 is a circuit diagram of an example of the balanced type DDA;
FIG. 3 is a circuit diagram of an example of a common mode feedback circuit in the balanced type DDA;
FIG. 4 is a circuit diagram of a conventional non-inverting amplifier circuit using the balanced type DDA;
FIG. 5 is a circuit diagram of a simple differential input stage constituting a DDA;
FIG. 6 is a graph showing characteristics of the differential input stage;
FIG. 7 is a circuit diagram of a multiple input circuit using a conventional balanced type DDA;
FIG. 8 is a circuit diagram of the first preferred embodiment of a differential amplifier circuit according to the present invention;
FIG. 9 is a circuit diagram of a single end type DDA of FIG. 8;
FIG. 10 is a circuit diagram of a non-inverting amplifier circuit using the differential amplifier circuit of FIG. 8;
FIG. 11 is a circuit diagram of the second preferred embodiment of a differential amplifier circuit according to the present invention; and
FIG. 12 is a circuit diagram of a multiple input circuit using the differential amplifier circuit of FIG. 11.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0029] Referring now to the accompanying drawings, the preferred embodiments of the present invention will be described below.

(First Preferred Embodiment)

[0030] FIG. 8 shows the first preferred embodiment of a differential amplifier circuit 3 according to the present invention. This differential amplifier circuit 3 comprises a balanced type DDA 1 and a single ended type DDA 2. The balanced type DDA 1 is the same as those shown in FIGS. 1 and 2, and has two differential input stages and a common mode feedback circuit. Four input terminals VPP, VPN, VNN and VNP of the DDA 1 are four input terminals of the differential amplifier circuit 3, and two output terminals VoutP and VoutN of the DDA 1 are two output terminals of the differential amplifier circuit 3.

[0031] In the balanced type DDA 1, an output signal from the output terminal VoutP has a first positive gain with respect to an input signal of a difference between the input terminal VPP and the input terminal VPN, and an output signal from the output VoutN has a second negative gain, the absolute value of which is substantially equal to that of the first gain. In addition, with respect to an input signal of a difference between the input terminal VNP and the input terminal VNN, an output signal from the output terminal VoutP has a third negative gain, the absolute value of which

is substantially equal to that of the first gain, and an output signal from the output terminal v_{outN} has a fourth positive gain, the absolute value of which is substantially equal to that of the third gain.

[0032] The single ended type DDA 2 has four input terminals corresponding to the four input terminals VPP, VPN, VNN and VNP of the balanced type DDA 1, and an output terminal Vco. Two input terminals VPP and VPN of the four input terminals of the single end type DDA 2 are connected to corresponding two input terminals VPP and VPN of the four input terminals of the balanced type DDA 1, respectively, whereas the remaining two input terminals VNN and VNP of the single end type DDA 2 are inversely connected to the remaining two input terminals VNP and VNN of the balanced type DDA 1, respectively. The output terminal Vco of the single end type DDA 2 serves as a control output terminal of the differential amplifier circuit 3. For example, the single ended type DDA 2 is formed as shown in FIG. 9. In this figure, one output stage 14 of the two output stages 13 and 14 of the balanced type DDA shown in FIG. 2, and the accompanying phase compensator circuit thereof are removed, and the common mode feedback circuit 15 is also removed. In addition, in PMOS transistors Q5 and Q6 which are loads of two differential input stages, the gate and drain of the transistor Q5 are connected to each other to form a PMOS current mirror load. Its one output terminal VoutN is a control output terminal Vco of the DDA 2.

[0033] In the single ended type DDA 2, the output signal of the output terminal Vco has a positive gain with respect to the input signal between the input terminals VPP and VPN, and the output signal of the output terminal Vco substantially has the same positive gain with respect to the input signal between the input terminals VNN and VNP.

[0034] FIG. 10 is a circuit diagram of a non-inverting amplifier circuit in this preferred embodiment, which uses the differential amplifier circuit 3 shown in FIG. 8. As shown in this figure, the input terminals VPP and VNP of the input terminals VPP, VPN, VNN and VNP of the differential amplifier circuit 3 serve as differential signal input terminals. The signal of one output terminal VoutP is negatively fed back to the input terminal VPN via a resistor R1, and the signal of the other output terminal VoutN is negatively fed back to the input terminal VNN via a resistor R2. The signal of the control output terminal Vco is negatively fed back to the input terminal VPN via a resistor R3a, and to the input terminal VNN via a resistor R3b.

[0035] By the negative feedback via the resistors R1 and R2, the non-inverting amplifier circuit in this preferred embodiment operates so as to satisfy the relationship expressed by the formula (1), similar to the conventional circuit, if the gain of the balanced type DDA 1 is infinity. On the other hand, since the negative feedback is carried out from the control output terminal Vco to the input terminals VPN and VNN via the resistors R3a and R3b, respectively, the following formula (14) is satisfied if the gain of the single end DDA 2 is infinity.

$$(VPP - VPN) + (VNP - VNN) = 0 \quad (14)$$

[0036] Because of simultaneously the formulae (1) and (14) is satisfied, the following conditions (15) and (16) are resulted.

$$VPP = VPN \quad (15)$$

$$VNP = VNN \quad (16)$$

[0037] Therefore, in the non-inverting amplifier circuit shown in FIG. 10, a virtual short-circuit is established between two input terminals of each differential input stages of the balanced type DDA 1 in the differential amplifier circuit 3, so the distortions are greatly suppressed. Assuming that the value of resistance of the resistors R3a and R3b is R_a and that the value of resistance of the resistors R1 and R2 is R_b , the gain of the non-inverting amplifier circuit is given by the following formula (17).

$$A = \{R_b + (R_a/2)\} / (R_a/2) \quad (17)$$

[0038] As described above, according to this preferred embodiment, even if the common mode component of the input signal of the balanced type DDA 1 is different from the common mode component of the output signal, it is possible to reduce distortion by incorporating the single ended type DDA 2 to carry out a negative feedback. In addition, unlike conventional circuits, it is not required to reduce the gain of the balanced type DDA in order to reduce distortion, so that it is possible to easily carry out a phase compensation, and to implement the desired transfer function with much greater accuracy with comparison to conventional one.

(Second Preferred Embodiment)

[0039] FIG. 11 shows the second preferred embodiment of a differential amplifier circuit 3a according to the present invention. Also in this preferred embodiment similar to the first preferred embodiment, a balanced type DDA 1 and a single ended type DDA 2 are used. However, the relationship between the connections of input terminals is opposite to that in FIG. 8. That is, two input terminals VNN and VNP of the four input terminals of the single ended type DDA 2 are connected to corresponding two input terminals VNN and VNP of the four input terminals of the balanced type DDA 1, respectively, whereas the remaining two input terminals VPP and VPN of the single end type DDA 2 are inversely connected to the remaining two input terminals VPN and VPP of the balanced type DDA 1, respectively.

[0040] FIG. 12 shows a multiple input circuit using the differential amplifier circuit 3a of FIG. 11. To the four input terminals VPP, VPN, VNN and VNP of the differential amplifier circuit 3a, input signals VinPP, VinPN, VinNN and VinNP are supplied via input resistors R5, R3, R4 and R6, respectively. Output terminals VoutP and VoutN are negatively fed to the input terminals VPN and VNN via resistors R1 and R2, respectively.

[0041] Also in this preferred embodiment, if the gain of the balanced type DDA 1 is infinity, the relationship expressed by the formula (1) is established similar to the preceding preferred embodiment. In addition, if the gain of the single ended type DDA 2 is infinity, the relationship expressed by the formula (14) is established similar to the preceding preferred embodiment. Therefore, similar to the preceding preferred embodiment, the relationship expressed by the formula (15) and (16) is established, and a virtual short-circuit is established between all of the input terminals of two differential input stages of the balanced type DDA 1, so the distortions are greatly suppressed. Assuming that the value of resistance of the resistors R3 and R4 is Ra, the value of resistance of the resistors R1 and R2 is Rb, the value of resistance of the resistors R5 and R6 is Rc, and the value of resistance of the resistors R7a and R7b is Rd/2, then, the output differential component Vo of this circuit is given by the formula (11) similar to the conventional circuit shown in FIG. 7.

$$V_o = \frac{(R_d / 2)(R_a + R_b)}{(R_c + R_d / 2)R_a} V_{iP} - \frac{R_b}{R_a} V_{iN} \quad (11)$$

[0042] While the resistors have been inserted into the feedback paths of the differential amplifier circuit 3 in the above described preferred embodiments, other feedback circuit elements or impedance elements, e.g., capacities, not resistors, may be inserted.

[0043] The amplifier circuit according to the present invention can form various feedback circuits in accordance with uses. For example, the amplifier circuit may comprise a feedback circuit for causing the output signal of a first output terminal to be negatively fed back to first and third differential input stages, a feedback circuit for causing the output signal of a second output terminal to be negatively fed back to second and fourth differential input stages, and a feedback circuit for causing the output signal of a third output terminal to be negatively fed back to the first through fourth differential input stages.

[0044] As described above, according to the present invention, by combining a balanced type DDA with a single end type DDA to carry out a feedback control so that a virtual short-circuit is established between two input terminals of each differential input stages, it is possible to obtain a differential amplifier circuit capable of reducing distortion without enlarging a linear region. By using this differential amplifier circuit, it is possible to form a non-inverting amplifier circuit and a subtracter circuit, which have high input impedance.

[0045] While the present invention has been disclosed in terms of the preferred embodiment in order to facilitate better understanding thereof, it should be appreciated that the invention can be embodied in various ways without departing from the principle of the invention. Therefore, the invention should be understood to include all possible embodiments and modification to the shown embodiments which can be embodied without departing from the principle of the invention as set forth in the appended claims.

Claims

1. An amplifier circuit comprising:

a first four-input balanced amplifier having

a first differential terminal pair and a second differential terminal pair;
a first output terminal and a second output terminal, output signals at the first output terminal and the second output terminal being complementary; and

a second four input single-ended amplifier having
a third differential terminal pair and a fourth differential terminal pair;
a third output terminal;
wherein the first differential terminal pair and the third differential terminal pair are connected in parallel, and
the second differential terminal pair and the fourth differential terminal pair are connected in reverse parallel.

2. The amplifier circuit according to claim 1, wherein the characteristics between the first output terminal and the first differential input pair, and those between the first output terminal and the second differential input pair are matched, and wherein the characteristics between the second output terminal and the first differential input pair, and those between the second output terminal and the second differential input pair are matched.

3. The amplifier circuit according to claim 2, wherein the characteristics between the third output terminal and the third differential input pair and those between the third output terminal and the fourth differential input pair are matched.

4. The amplifier circuit according to claim 3, further comprising:

a first circuit for connecting the first output with the first differential input pair;
a second circuit connecting the second output with the second differential input pair;
wherein characteristics of said first circuit and said second circuit are matched.

5. The amplifier circuit according to claim 4, further comprising:

a third circuit for connecting the third output with the third differential input pair;
a fourth circuit for connecting the third output with the fourth differential pair;
wherein characteristics of said third circuit and said fourth circuit are matched.

6. The amplifier circuit according to claim 5, wherein said first, second, third and fourth circuits create negative feedback loops.

7. An amplifier circuit comprising:

a first four-input balanced amplifier having

a first differential terminal pair and a second differential terminal pair;
a first output terminal and a second output terminal, output signals at the first output terminal and the second output terminal being complementary; and

a second four input single-ended amplifier having

a third differential terminal pair and a fourth differential terminal pair;
a third output terminal;

wherein the first differential terminal pair and the third differential terminal pair are connected in reverse parallel, and the second differential terminal pair and the fourth differential terminal pair are connected in parallel.

8. The amplifier circuit according to claim 7, wherein the characteristics between the first output terminal and the first differential input pair, and those between the first output terminal and the second differential input pair are matched, and wherein the characteristics between the second output terminal and the first differential input pair, and those between the second output terminal and the second differential input pair are matched.

9. The amplifier circuit according to claim 8, wherein the characteristics between the third output terminal and the third differential input pair and those between the third output terminal and the fourth differential input pair are matched.

10. The amplifier circuit according to claim 9, further comprising:

a first circuit for connecting the first output with the first differential input pair;
a second circuit for connecting the second output with the second differential input pair;

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wherein characteristics of said first circuit and said second circuit are matched.

11. The amplifier circuit according to claim 10, further comprising:

5 a third circuit for connecting the third output with the third differential input pair;
 a fourth circuit for connecting the third output with the fourth differential pair;
 wherein characteristics of said third circuit and said fourth circuit are matched.

10 12. The amplifier circuit according to claim 11, wherein said first, second, third and fourth circuits create negative
 feedback loops.

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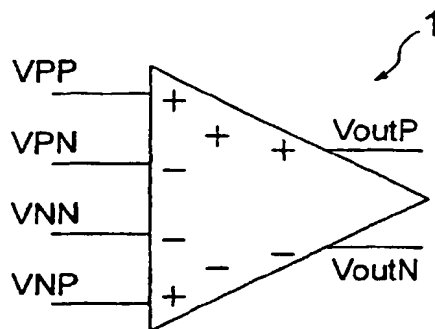


FIG. 1

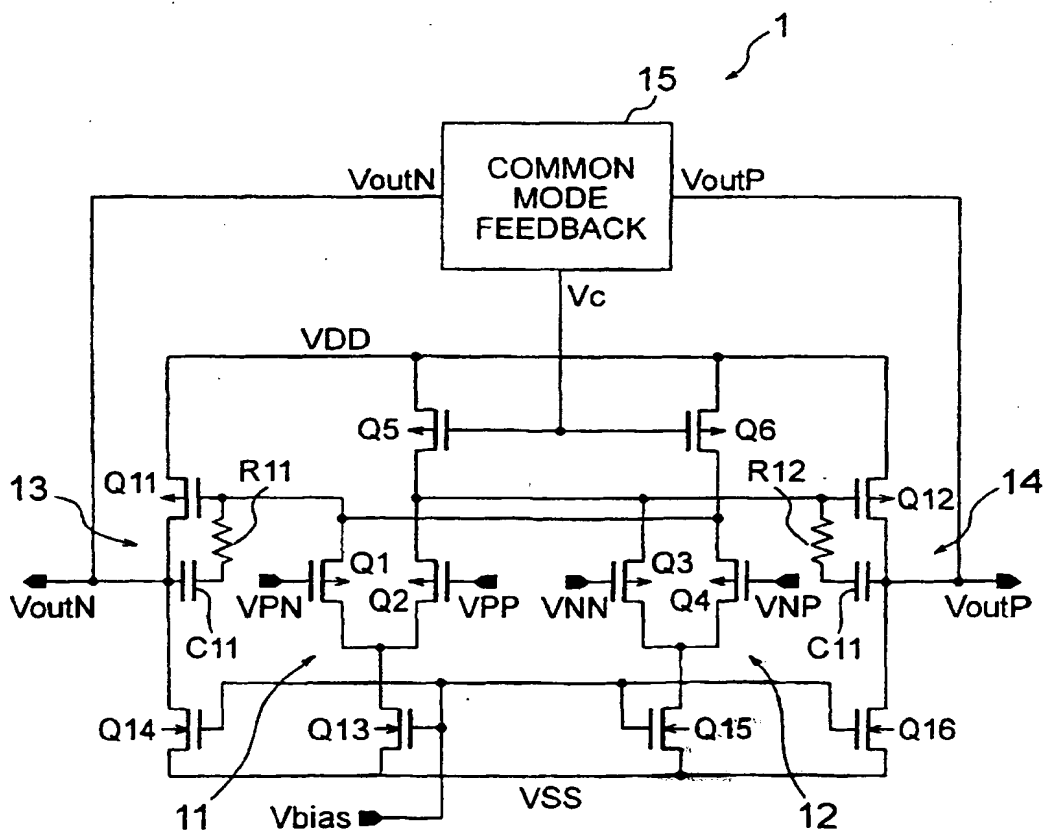


FIG. 2

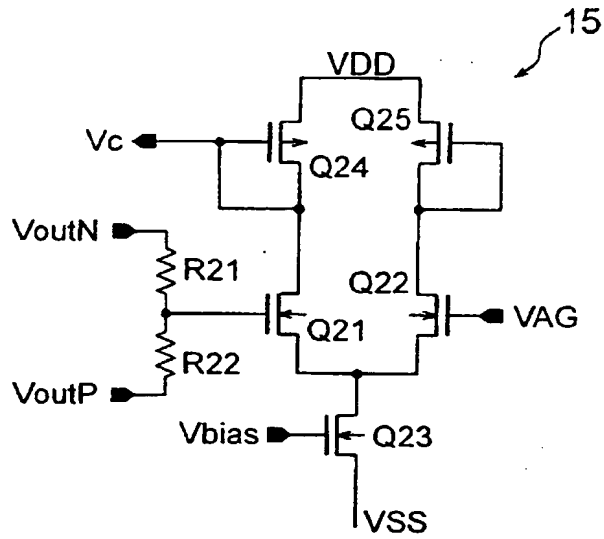


FIG. 3

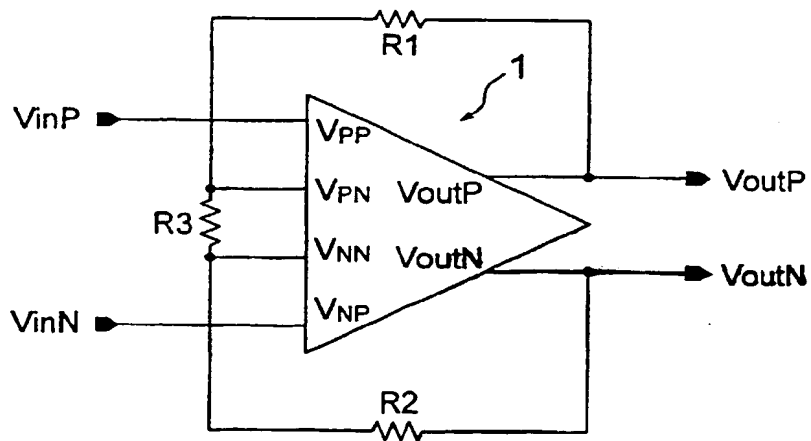


FIG. 4

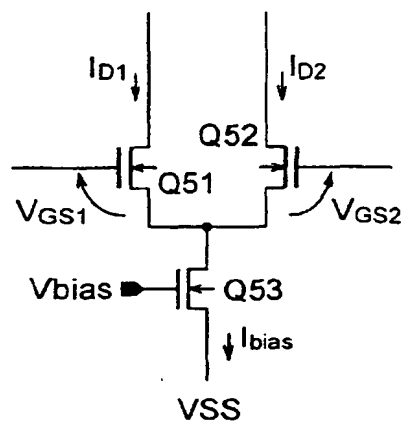


FIG. 5

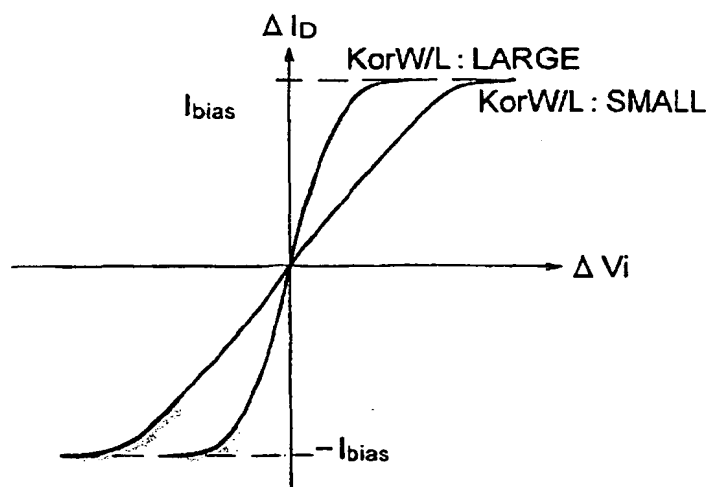


FIG. 6

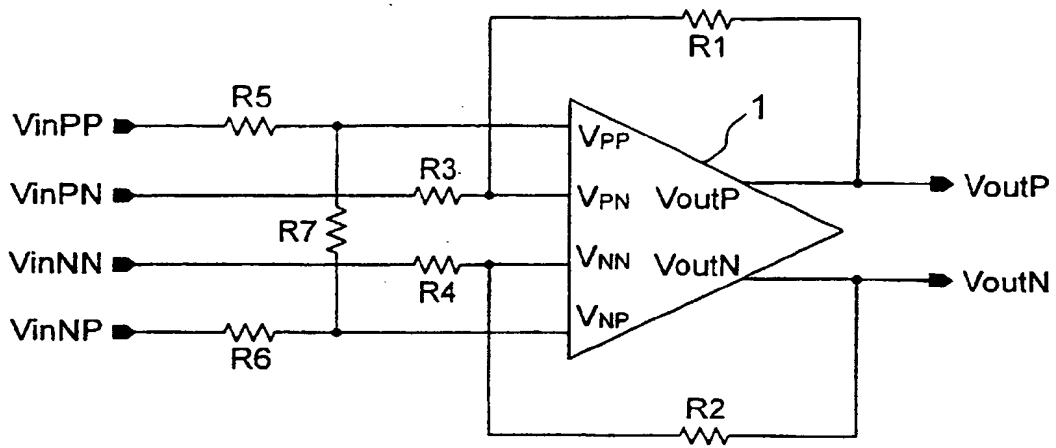


FIG. 7

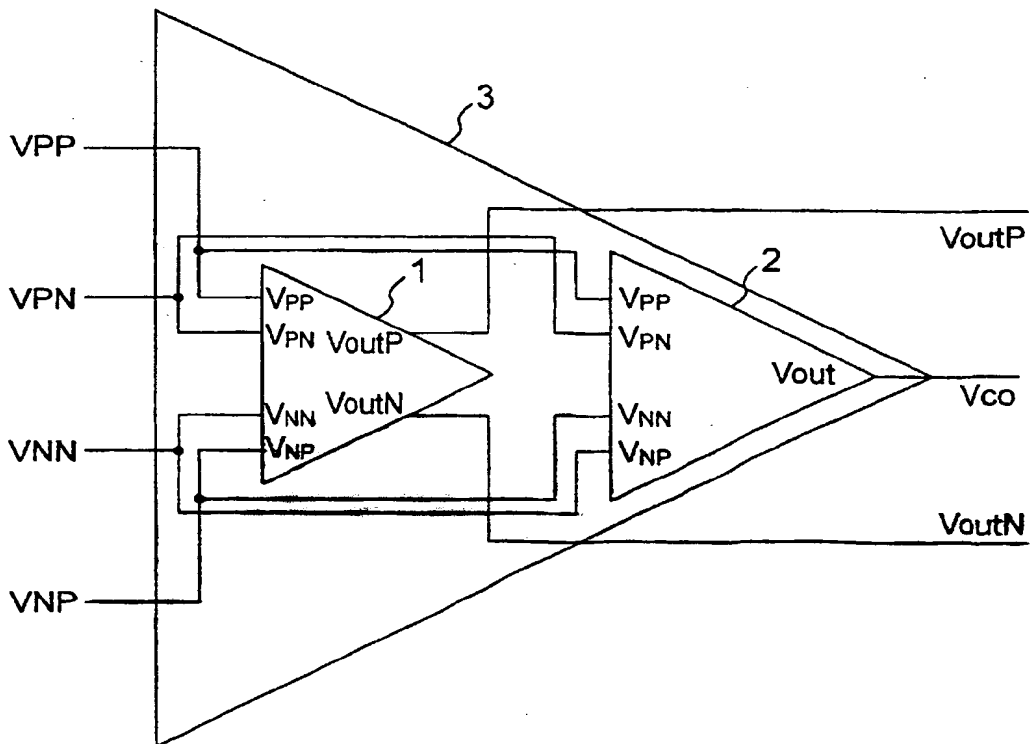


FIG. 8

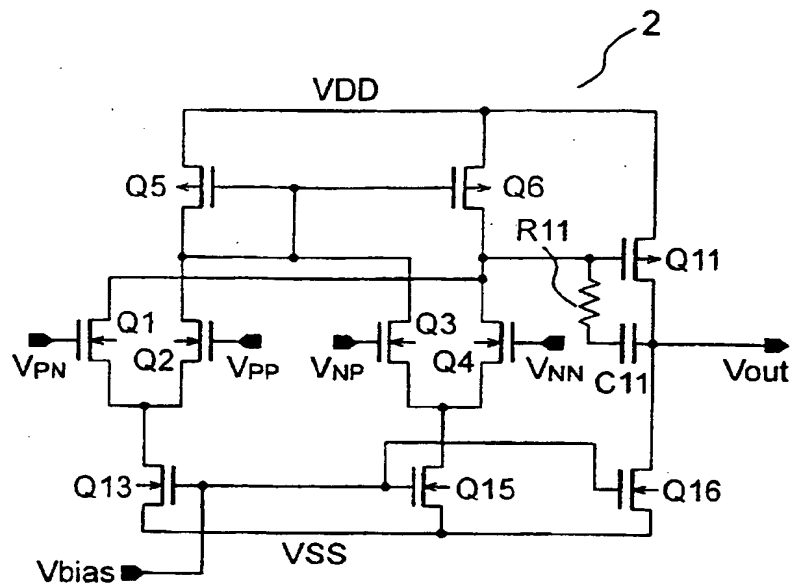


FIG. 9

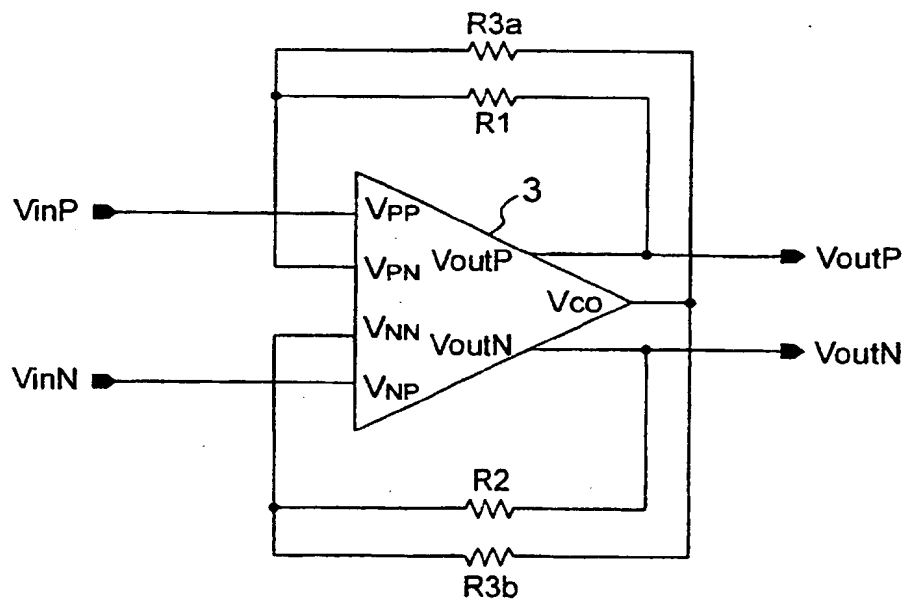


FIG. 10

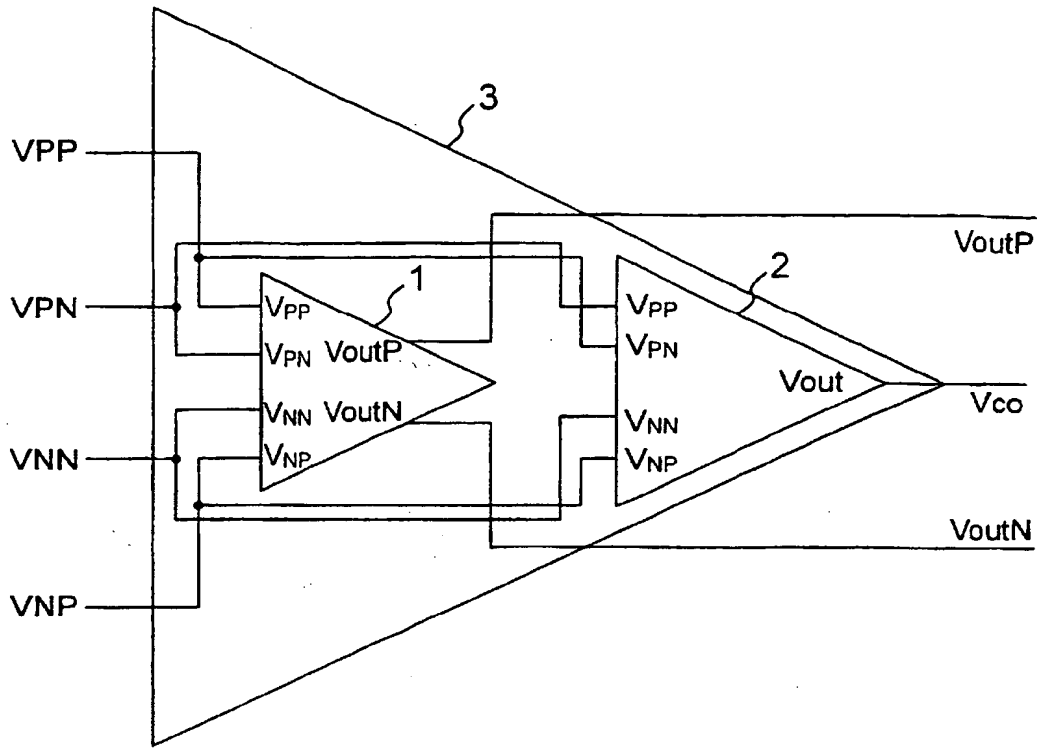


FIG. 11

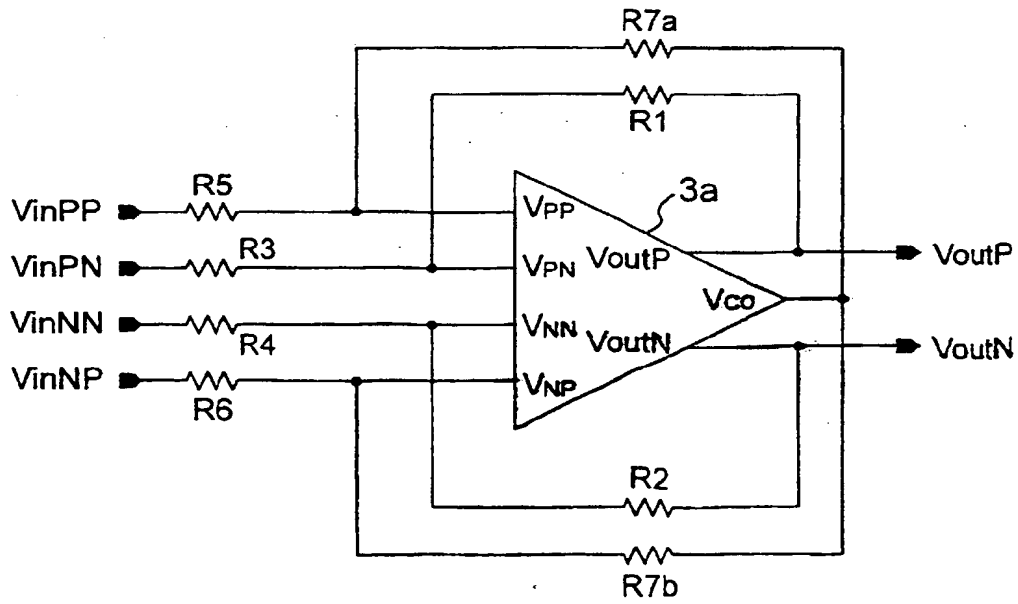


FIG. 12